CLAIMS:

1. A method for forming, in accordance with a definition file, a parallel processing system that includes a plurality of types of elements that operate in parallel,

the definition file including a plurality of parallel descriptions that respectively define a plurality of parallel processes performed independently, the plurality of parallel descriptions including a first parallel description showing a first parallel process with a plurality of data inputs including at least one data input into which output data of another parallel process is inputted,

and the method comprising:

a first step of generating, based on a hardware library in which information on the plurality of types of elements is stored, hardware configuration information including circuit configurations for executing the parallel processes defined by the parallel descriptions of the definition file, the circuit configurations including at least one of the plurality of types of elements; and

a second step of adding a delay element to the hardware configuration information so that data with a same latency from input into the parallel processing system are inputted into a plurality of data inputs of a circuit configuration for executing the first parallel process.

2. The method for forming according to Claim 1, wherein the parallel processing system is reconfigurable to different hardware configurations by changing connections between the plurality of types of elements and the hardware configuration information includes information showing a plurality of different hardware configurations.

3. The method for forming according to Claim 1, wherein the plurality of types of elements include a plurality of types of operation units of a scale whereby one operation unit is capable of processing parallel process defined by one parallel description of the definition file.

4. The method for forming according to Claim 1, wherein the plurality of types of elements include a plurality of types of operation units for executing different operations in byte or word units.

5. The method for forming according to Claim 1, wherein information on a number of cycles consumed by respective types of elements is stored in the hardware library, and

in the second step, the delay element corresponding to a number of cycles consumed by at least one of the plurality of types of elements is added.

6. The method for forming according to Claim 1, wherein the plurality of parallel descriptions include a second parallel description that defines a second parallel process including shared processing that is common to at least part of a third parallel process defined by a third parallel description,

in the first step, a shared circuit configuration including at least one of the plurality of types of elements is generated for the shared processing, and

in the second step, the delay element is added to a circuit configuration for executing a difference between the second parallel process and the shared processing as the circuit configuration for executing the first parallel process.

7. An apparatus for forming, in accordance with a definition file, a parallel processing system that includes a plurality of types of elements that operate in parallel,

the definition file including a plurality of parallel descriptions that respectively define a plurality of parallel processes performed independently, the plurality of parallel descriptions including a first parallel description showing a first parallel process with a plurality of data inputs including at least one data input into which output data of another parallel process is inputted,

the apparatus comprising:

a first means for generating, based on a hardware library in which information on the plurality of types of elements is stored, hardware configuration information including circuit configurations for executing the parallel processes defined by the parallel descriptions of the definition file, the circuit configurations including at least one of the plurality of types of elements; and

a second means for adding a delay element to the hardware configuration information so that data with a same latency from input into the parallel processing system are inputted into a plurality of data inputs of a circuit configuration for executing the first parallel process.

8. The apparatus according to Claim 7, wherein the parallel processing system is reconfigurable to different hardware configurations by changing connections between the plurality of types of elements and the hardware configuration information includes information showing a plurality of different hardware configurations.

9. A program product for causing a computer to execute a process for designing, in accordance with a definition file, a system that includes a plurality of types of elements that operate in parallel,

the definition file including a plurality of parallel descriptions that respectively define a plurality of parallel processes performed independently, the plurality of parallel descriptions including a first parallel description showing a first parallel process with a plurality of data inputs including at least one data input into which output data of another parallel process is inputted,

the process for designing comprising:

a first step of generating, based on a hardware library in which information on the plurality of types of elements is stored, hardware configuration information including circuit configurations for executing the parallel processes defined by the parallel descriptions of the definition file, the circuit configurations including at least one of the plurality of types of elements; and

a second step of adding a delay element to the hardware configuration information so that data with a same latency from input into the parallel processing system are inputted into a plurality of data inputs of a circuit configuration for executing the first parallel process.

10. A computer-readable recording medium on which a definition file is stored, the definition file including a plurality of parallel descriptions that respectively define a plurality of parallel processes performed independently and in synchronization by a system that includes a plurality of elements that operate in parallel, the plurality of parallel descriptions including a first parallel description showing a first parallel process with a plurality of data inputs including at least one data input into which output data of another parallel process is inputted and showing that data with a same latency from input into the system are inputted into the plurality of data inputs.

11. The recording medium according to Claim 10, wherein the plurality of parallel descriptions respectively define a plurality of parallel processes to be executed in synchronization with a clock for operations by the plurality of elements.

12. A method of simulating, based on a definition file, a system that includes a plurality of types of elements that operate in parallel,

the definition file including a plurality of parallel descriptions that respectively define a plurality of parallel processes preformed independently, the plurality of parallel descriptions including a first parallel description showing a first parallel process with a plurality of data inputs including at least one data input into which output data of another parallel process is inputted,

the method comprising a step of executing a plurality of parallel processes defined by the definition file in synchronization, wherein in the step of executing, data with a same latency from input in the system are inputted into the plurality of data inputs of the first parallel process.

13. A simulator for simulating, based on a definition file, a system that includes a plurality of types of elements that operate in parallel,

the definition file including a plurality of parallel descriptions that respectively define a plurality of parallel processes performed independently, the plurality of parallel descriptions including a first parallel description showing a first parallel process with a plurality of data inputs including at least one data input into which output data of another parallel process is inputted,

the simulator comprising a means of executing a plurality of parallel processes defined by the definition file in synchronization, wherein in the means of executing, data with a same latency from input in the system are inputted into the plurality of data inputs of the first parallel process.

14. A program product for causing a computer to simulate, based on a definition file, a system that includes a plurality of types of elements that operate in parallel,

the definition file including a plurality of parallel descriptions that respectively define a plurality of parallel processes preformed independently, the plurality of parallel descriptions including a first parallel description showing a first parallel process with a

plurality of data inputs including at least one data input into which output data of another parallel process is inputted,

wherein when the computer simulates a step of executing a plurality of parallel processes defined by the definition file in synchronization, data with a same latency from input in the system are inputted into the plurality of data inputs of the first parallel process.